CLAIMS

1. A computer system, comprising:

a first processor;

a second processor for use as a coprocessor to the first processor;

a coprocessor controller;

a memory; and

a decoupling element;

wherein instructions are passed to the second processor from the first processor through the decoupling element, such that the second processor consumes instructions derived from the first processor through the decoupling element, wherein the second processor receives data from and writes data to the memory, and wherein the coprocessor controller controls the activity of the second processor to ensure execution of the coprocessor is correctly ordered with respect to loads from memory, whereby the processing of instructions by the second processor is decoupled from the operation of the first processor.

2. A computer system as claimed in claim 1, wherein the decoupling element is a coprocessor instruction queue, wherein instructions are added to the coprocessor instruction queue by the first processor and consumed from the coprocessor instruction queue by the coprocessor.

3. A computer system as claimed in claim 1, wherein the decoupling element is a state machine, wherein information to provide instructions to the second processor is provided to the state machine by the first processor, and instructions are provided in an ordered sequence to the second processor by the state machine.

4. A computer system as claimed in claim 1, wherein the decoupling element is a third processor, wherein information to provide instructions to the second processor is provided to the third processor by the first processor, and instructions are provided in an ordered sequence to the second processor by the third processor.

5. A computer system as claimed in ~~any preceding~~ claim 1, wherein the second processor is configurable.

6. A computer system as claimed in claim 5, wherein the second processor is adapted to be configured in accordance with a configuration downloaded from the memory.

7. A computer system as claimed in ~~any preceding~~ claim 1, wherein the first processor is able to switch tasks during execution of instructions by the second processor.

8. A computer system as claimed in ~~any preceding~~ claim 1, further comprising a buffer memory from which the second processor loads data and to which the second processor stores data, wherein the buffer memory is adapted to load data from the memory and store data to the memory.

9. A computer system as claimed in claim 8, wherein the memory is dynamic random access memory, and the buffer memory is adapted to load data from, or store data to, the buffer memory in bursts.

10. A computer system as claimed in claim 8 ~~or claim 9~~, further comprising a second decoupling element, wherein memory instructions relating to movement of data between the buffer memory and the memory are passed to the buffer memory from the first processor through the second decoupling element, such that the buffer memory consumes instructions derived from the first processor through the second decoupling element, whereby the processing

of memory instructions by the buffer memory is decoupled from the operation of the first processor.

11. A computer system as claimed in claim 10, wherein the second decoupling element is a buffer memory instruction queue, wherein memory instructions are added to the buffer memory instruction queue by the first processor and consumed from the buffer memory instruction queue by the buffer memory.

12. A computer system as claimed in claim 10, wherein the second decoupling element is a state machine, wherein information to provide memory instructions to the buffer memory is provided to the state machine by the first processor, and memory instructions are provided in an ordered sequence to the buffer memory by the state machine.

13. A computer system as claimed in claim 10, wherein the second decoupling element is a fourth processor, wherein information to provide memory instructions to the buffer memory is provided to the fourth processor by the first processor, and memory instructions are provided in an ordered sequence to the buffer memory by the fourth processor.

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14. A computer system as claimed in any of claims 8 ~~to 13~~, further comprising a synchronisation mechanism to synchronise transfer of data between the buffer memory and the memory with execution of instructions by the second processor.

15. A computer system as claimed in claim 14, wherein the synchronisation mechanism is adapted to block execution of instructions by the second processor on data which has not yet been loaded to the buffer memory from the memory, and is adapted to block execution memory instructions for storage of data from the buffer memory to the memory where relevant instructions have not yet been executed by the second processor.

16. A computer system as claimed in claim 15, adapted such that when execution of instructions or memory instructions is blocked by the synchronisation mechanism, other instructions or memory instructions which are not blocked by the synchronisation mechanism may be carried out.

17. A computer system as claimed in ~~any previous~~ claim 1, wherein the first processor is the central processing unit of a computer device.

18. A method of operating a computer system, comprising:

providing code for execution by a first processor and a second processor acting as coprocessor to the first processor;

identification of a part of the code as providing a task to be carried out by the second processor;

passing information defining the task from the first processor to a decoupling element;

passing instructions derived from said information from the decoupling element to the second processor and executing said instructions on the second processor, wherein the processing of said instructions by the second processor is decoupled from the operation of the first processor.